



SKYLAKE-S V:1.0

ECS
CONFIDENTIAL

HSIO Lane Assignments by SKU (Lanes 1-14)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---------------------|---------|---------|---------|---------|---------|---------|---------|---------|----------|---------|---------|---------|---------|
| USB3 #1 (Dual-Mode) | USB3 #2 | USB3 #3 | USB3 #4 | USB3 #5 | USB3 #6 | USB3 #7 | USB3 #8 | USB3 #9 | USB3 #10 | PCIe #5 | PCIe #6 | PCIe #7 | PCIe #8 |
| | SSIC #1 | SSIC #2 | | | | GdE | PCIe #4 | PCIe #3 | PCIe #2 | PCIe #1 | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| X4 | | | | | | | | | | X4 | | | |
| | | | | | | X2 | | X2 | | X2 | | X2 | |
| | | | | | | N/A | | | | | | | |

| sku | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|------|----------|-----------|-----------|------|------|------|------|-----------|-----------|-----------|----------|------|------|------|
| H110 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | N/A | N/A | N/A | N/A | N/A | LAN Only | PCIe/LAN | PCIe | PCIe | PCIe |
| B150 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | USB3 | USB3 | N/A | N/A | N/A | LAN Only | PCIe/LAN | PCIe | PCIe | PCIe |
| Q150 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | USB3 | USB3 | USB3 | USB3 | N/A | LAN Only | PCIe/LAN | PCIe | PCIe | PCIe |
| H170 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | USB3 | USB3 | USB3 | USB3 | PCIe | PCIe/LAN | PCIe/LAN | PCIe | PCIe | PCIe |
| Z170 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | USB3 | USB3 | USB3 | USB3 | PCIe | PCIe/LAN | PCIe/LAN | PCIe | PCIe | PCIe |
| Q170 | USB3/OTG | USB3/SSIC | USB3/SSIC | USB3 | USB3 | USB3 | PCIe | USB3/PCIe | USB3/PCIe | USB3/PCIe | PCIe/LAN | PCIe | PCIe | PCIe |

HSIO Lane Assignments by SKU (Lanes 15-26)

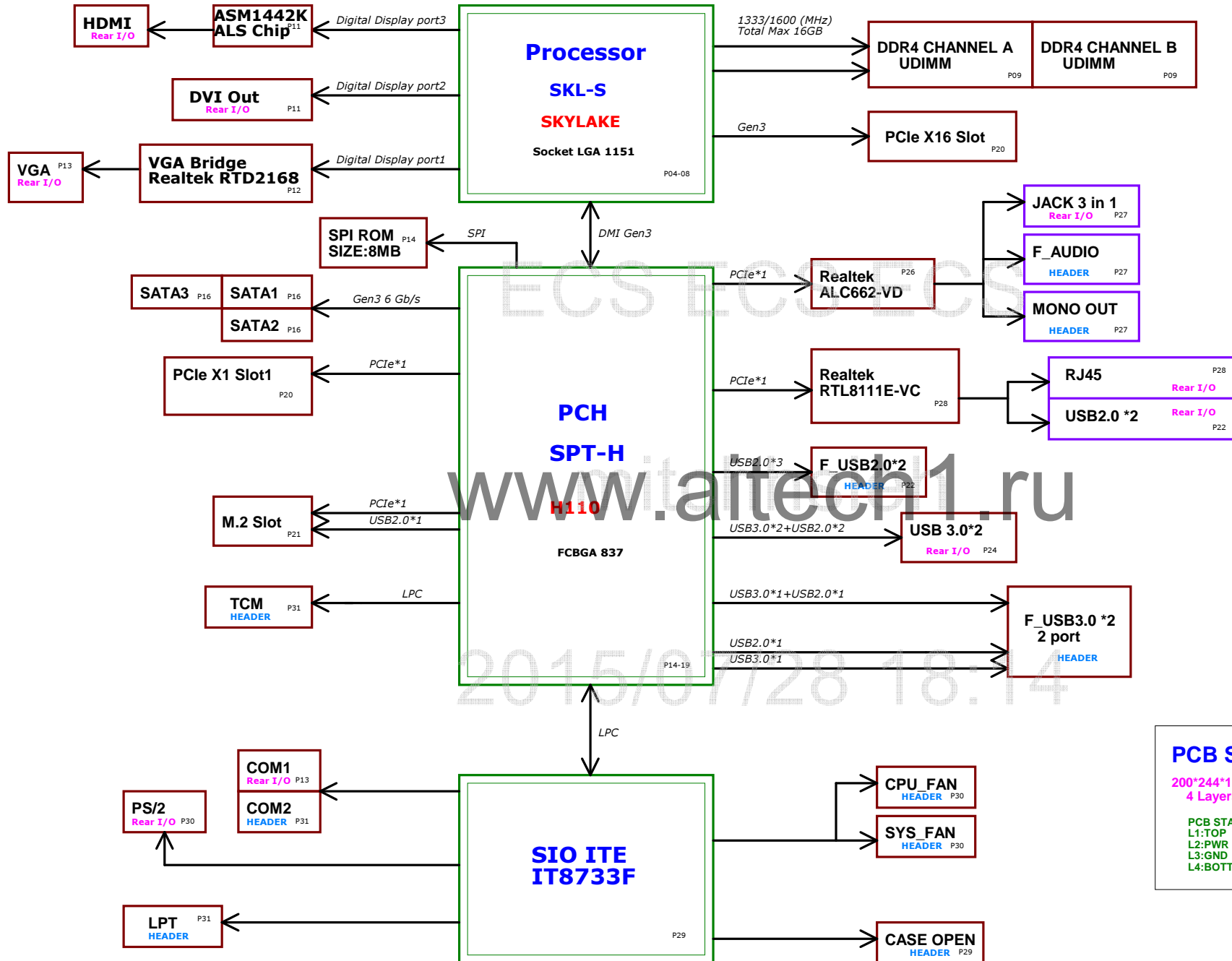
| 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 |
|-----------------------------|----------|----------|----------|-----------------------------|-----------|----------|----------|-----------------------------|----------|----------|----------|
| PCIe #9 | PCIe #10 | PCIe #11 | PCIe #12 | PCIe #13 | PCIe #14 | PCIe #15 | PCIe #16 | PCIe #17 | PCIe #18 | PCIe #19 | PCIe #20 |
| SATA #0 | SATA #1 | | | SATA #0** | SATA #1** | SATA #2 | SATA #3 | SATA #4 | SATA #5 | | |
| GbE | | | | GbE | | | | | | | |
| X4 | | | | X4 | | | | X4 | | | |
| X2 | | X2 | | X2 | | X2 | | X2 | | X2 | |
| Intel® RST for PCIe Storage | | | | Intel® RST for PCIe Storage | | | | Intel® RST for PCIe Storage | | | |

| sku | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | RST for PCIe Ports |
|------|----------|-------------|------|----------|------------|------------|------|------|------|------|------|------|--------------------|
| H110 | PCIe/LAN | PCIe | N/A | LAN Only | SATA*/LAN | SATA* | SATA | SATA | N/A | N/A | N/A | N/A | 0 |
| B150 | PCIe/LAN | PCIe*/SATA* | PCIe | PCIe/LAN | SATA*/LAN | SATA* | SATA | SATA | SATA | SATA | N/A | N/A | 0 |
| Q150 | PCIe/LAN | PCIe*/SATA | PCIe | PCIe/LAN | PCIe*/SATA | PCIe*/SATA | SATA | SATA | SATA | SATA | N/A | N/A | 0 |
| H170 | PCIe/LAN | PCIe*/SATA | PCIe | PCIe/LAN | PCIe*/SATA | PCIe*/SATA | SATA | SATA | SATA | SATA | PCIe | PCIe | 2 |
| Z170 | PCIe/LAN | PCIe*/SATA | PCIe | PCIe/LAN | PCIe*/SATA | PCIe*/SATA | SATA | SATA | SATA | SATA | PCIe | PCIe | 3 |
| Q170 | PCIe/LAN | PCIe*/SATA | PCIe | PCIe/LAN | PCIe*/SATA | PCIe*/SATA | SATA | SATA | SATA | SATA | PCIe | PCIe | 3 |

SCHEMATICS TABLE:

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| 19 | PCH-PWR | 41 | DC/DC VCCIO |
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Skylake-S Desktop Platform



PCB SIZE

200*244*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PW/R
L3:GND
L4:BOTTOM

PCH-GPIO function

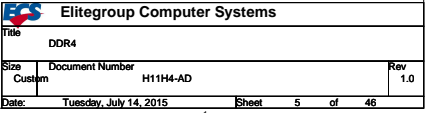
| Pin Name | Power Well | Usage | Default Status |
|----------|------------|--------------------------|--|
| GPP_F17 | 3VSB | LPC_PME_L | PME# GPI |
| GPD10 | ATX_3VSB | GPD10 (GPD10_DIS_ME) | GPD10 OUTPUT Low/Normal, High/ME disable |
| GPP_B13 | N/A | PCH_PLTRST_L | PLTRST# |
| GPP_G16 | N/A | GPP_G16 | GPO S0/S3/S4/S5:High |
| GPP_G15 | VCC3 | GPP_G15 (TMP Header Sel) | GPI |
| GPP_G13 | VCC3 | HDPANEL_DETECT | GPI |
| GPP_E7 | VCC3 | THERMAL_SD | GPI |
| GPP_B3 | VCC3 | BT_DIS_L_R | GPO S0/S3/S4/S5:High |
| GPP_H18 | 3VSB | GPP_H18 | GPI |
| GPP_H17 | 3VSB | GPP_H17 | GPI |
| GPP_H16 | 3VSB | GPP_H16 | GPI |
| GPP_H15 | 3VSB | GPP_H15 | For Acer Reserve |
| GPP_H14 | 3VSB | GPP_H14 | For Acer Reserve |
| GPP_B14 | +VCC3 | PCH_SPKR | SPKR |
| GPP_A14 | 3VSB | LPCPD_L | SUS_STAT# |
| GPP_C6 | 3VSB | SML1_CLK | SML1CLK |
| GPP_C7 | 3VSB | SML1_DATA | SML1DATA |
| GPP_E8 | VCC3 | SATALED_L | SATALED# |
| GPP_E9 | 3VSB | GPP_E9 (BIOS WP) | GPI INPUT Low/Normal, High/BIOS WP |
| GPP_E10 | 3VSB | GPP_E10 (SW BIOS WP) | GPO OUTPUT Low/BIOS WP, High/Normal |
| GPP_E0 | VCC3 | GPP_E0 (OBR) | GPI |
| GPP_E4 | VCC3 | GPP_E4 | GPO S0/S3/S4/S5:High |
| GPP_F22 | VCC3 | PCH_GPP_F22 (PCIEX16RST) | GPO S0:High S3/S4/S5:Low |
| GPP_F16 | 3VSB | GPP_F16 (USB_EN) | GPO S0/S3:High S4/S5:Low |
| GPP_F14 | 3VSB | H_SKTOCC_L | GPI |
| GPP_B17 | VCC3 | M.2_DIS_L_R | GPO S0/S3/S4/S5:High |
| GPP_B6 | VCC3 | CLK_REQ1_M.2_WLAN_L | GPO |
| GPP_B8 | VCC3 | GPP_B8 | GPI |
| GPD0 | DSW | RLAN_PWR_EN | GPO |
| GPP_D4 | 3VSB | SIO_GP16(PC_health) | GPI |

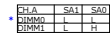
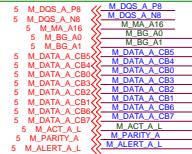
SIO-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|--------------|---------------------|-------------------|
| GP37 | +DIMM_5VDUAL | SIO_LED1 | FAN_TAC3(DI) |
| GP36 | 3VSB | THERMAL_SD | FAN_CTL3(DOD8) |
| GP35 | +DIMM_5VDUAL | SIO_LED0 | FAN_TAC4(DI) |
| GP34 | 3VSB | SUSWARN_L | SUSWARN#(DOD8) |
| GP33 | 3VSB | SUSACK_L | SUSACK#(DOD8) |
| GP32 | ATX3VSB | DPWROK | DPWROK(DOD8) |
| GP30 | VCC | ATX_PWRGD | ATXPG(DI) |
| GP14 | 3VSB | SML1_CLK | VCORE_EN(DOD8) |
| N/A | 3VSB | SML1_DATA | PCH_D1 |
| GP13 | VCC3 | PCH_SYSPWROK | PWROK1(DOD8) |
| GP12 | N/A | PCIRST1_L | PCIRST1#(DO8) |
| GP11 | N/A | PCIRST2_L | PCIRST2#(DO8) |
| GP44 | 3VSB | SIO_PWRON_L | PWRON#(DOD8) |
| GP54 | 3VSB | LPC_PME_L | PME#(DOD8) |
| GP43 | ATX5VSB | FP_PWRBTN_L | PANSWH#(DI) |
| GP42 | ATX3VSB | ATX_PSON_L | PSON#(DOD8) |
| GP53 | N/A | SLP_S4_L | SUSC#(DI) |
| GP40 | 3VSB | 3VBSBW_L | 3VBSBW#(DO8) |
| GP10 | N/A | PCIRST3_L | PCIRST3#(DO8) |
| GP55 | 3VSB | RSMRST_L | RSMRST3#(DOD8) |
| GP16 | 3VSB | SIO_GP16(PC_health) | 5VSB_CTRL3#(DOD8) |

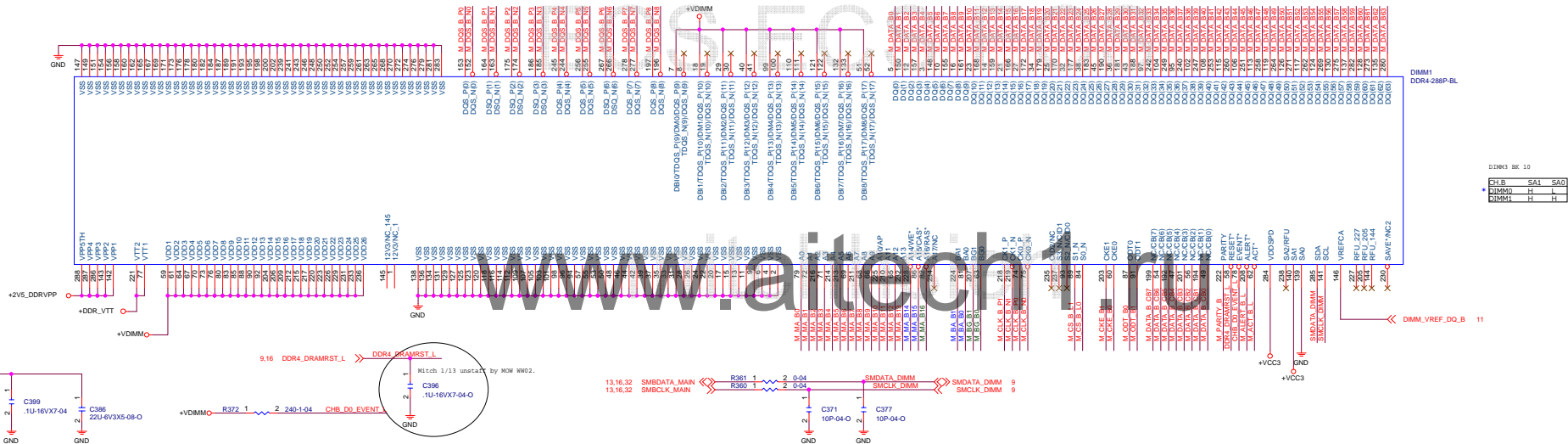
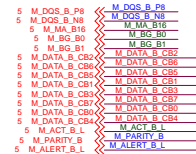
CPU-Strap

| Pin Name | Usage | Default Status |
|-----------------------|---|---|
| CFG0 | CFG[0]: Stall reset sequence after PCU PL lock until deasserted | 1 = (Default) Normal Operation |
| CFG1 | CFG[1]: Reserved configuration lane | |
| CFG2:5:6 | CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express | PCIE16X |
| CFG3 | CFG[3]: Reserved configuration lane. | |
| CFG4 | CFG[4]: eDP enable: | 1 = Disabled. |
| CFG7 | CFG[7]: PEG Training: | 1 = (default) PEG Train immediately following RESET# deassertion. |
| CFG19:8 | CFG[19:8]:Reserved configuration lanes. | |
| SPKR/GPP_B14 | Top Swap Override | 0 =Disable "Top Swap" mode. (Default) |
| GSPI0_MOSI/GPP_B18 | No Reboot | 0 =Disable "No Reboot" mode |
| SMBALERT#/GPP_C2 | TLS Confidentiality | 1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS |
| GSPI1_MOSI/GPP_B22 | Boot BIOS Strap Bit BBS | 0=SPI |
| SML0ALERT#/GPP_C5 | eSPI or LPC | 0 =LPCIs selected for EC. |
| HDA_SDO | Flash Descriptor Security Override | This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. |
| DDPB_CTRLDATA/GPP_I6 | Display Port B Detected | 1 = Port B is detected. |
| DDPC_CTRLDATA/GPP_I8 | Display Port C Detected | 1 = Port C is detected. |
| DDPB_CTRLDATA/GPP_I10 | Display Port D Detected | 1 = Port D is detected. |

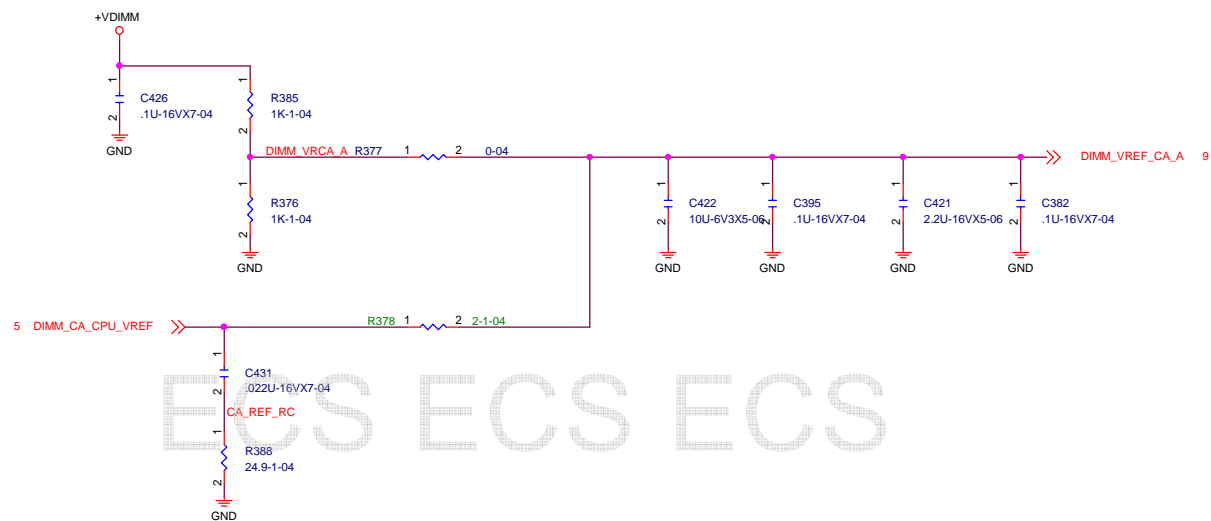




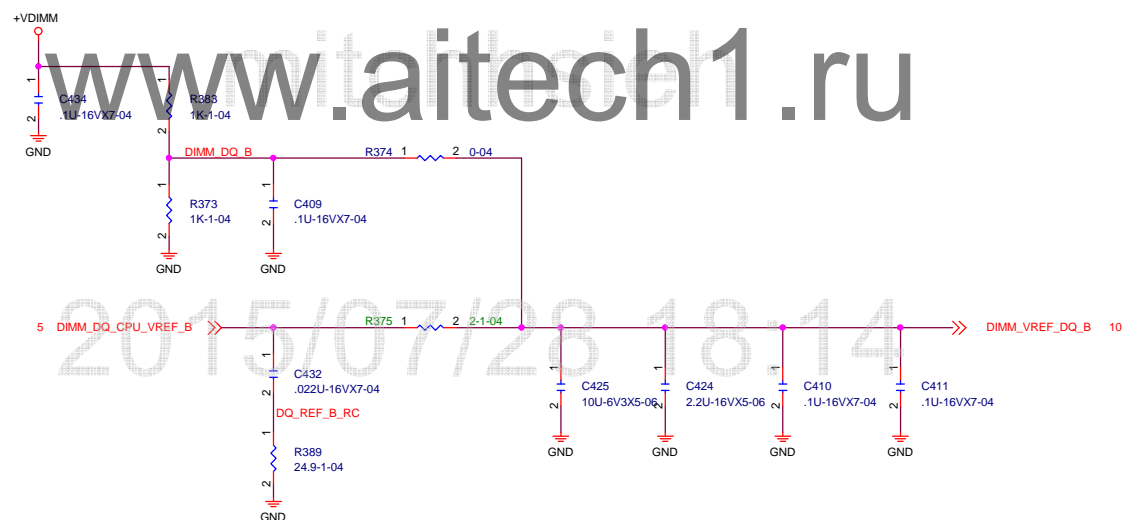
DDR3L CH.B



DIMM_VREF_CA



DIMM_VREF_DQ

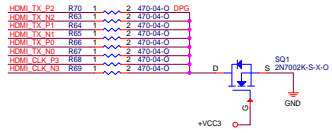


| Pin#2 | DDI2_TXP[0] | DDI2_LANE1_DP | HDMDX_TX2_DP |
|-------|-------------|---------------|--------------|
| | DDI2_TXN[0] | DDI2_LANE1_DN | HDMDX_TX2_DN |
| | DDI2_TXP[1] | DDI2_LANE1_DP | HDMDX_TX1_DP |
| | DDI2_TXN[1] | DDI2_LANE1_DN | HDMDX_TX1_DN |
| | DDI2_TXP[2] | DDI2_LANE2_DP | HDMDX_TX0_DP |
| | DDI2_TXN[2] | DDI2_LANE2_DN | HDMDX_TX0_DN |
| | DDI2_TXP[3] | DDI2_LANE3_DP | HDMDX_CLK_DP |
| | DDI2_TXN[3] | DDI2_LANE3_DN | HDMDX_CLK_DN |

HDMI

HDMI-DDI TX0/TX1/TX2 6pin交叉表

| | | | | | |
|--------------|-----|---|---|---------------|-------------|
| 4 DDI2_TX_N3 | C84 | 1 | 2 | 1U-18VX7-04-O | HDMI_CLK_N3 |
| 4 DDI2_TX_P3 | C83 | 1 | 2 | 1U-18VX7-04-O | HDMI_CLK_P3 |
| 4 DDI2_TX_N2 | C82 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_N2 |
| 4 DDI2_TX_P2 | C81 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_P2 |
| 4 DDI2_TX_N1 | C80 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_N1 |
| 4 DDI2_TX_P1 | C79 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_P1 |
| 4 DDI2_TX_N0 | C78 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_N0 |
| 4 DDI2_TX_P0 | C77 | 1 | 2 | 1U-18VX7-04-O | HDMI_TX_P0 |

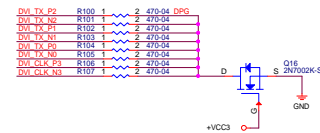


DVI

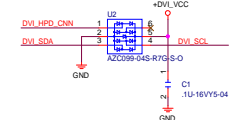
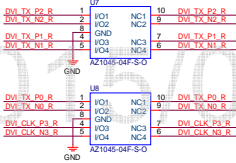
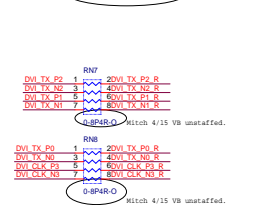
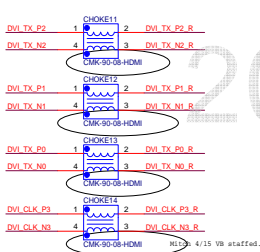
| Pin#2 | DDI2_TXP[0] | DDI2_LANE1_DP | HDMDX_TX2_DP |
|-------|-------------|---------------|--------------|
| | DDI2_TXN[0] | DDI2_LANE1_DN | HDMDX_TX2_DN |
| | DDI2_TXP[1] | DDI2_LANE1_DP | HDMDX_TX1_DP |
| | DDI2_TXN[1] | DDI2_LANE1_DN | HDMDX_TX1_DN |
| | DDI2_TXP[2] | DDI2_LANE2_DP | HDMDX_TX0_DP |
| | DDI2_TXN[2] | DDI2_LANE2_DN | HDMDX_TX0_DN |
| | DDI2_TXP[3] | DDI2_LANE3_DP | HDMDX_CLK_DP |
| | DDI2_TXN[3] | DDI2_LANE3_DN | HDMDX_CLK_DN |

HDMI-DDI TX0/TX1/TX2 6pin交叉表

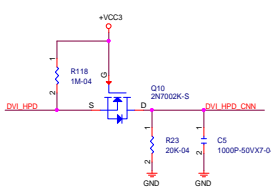
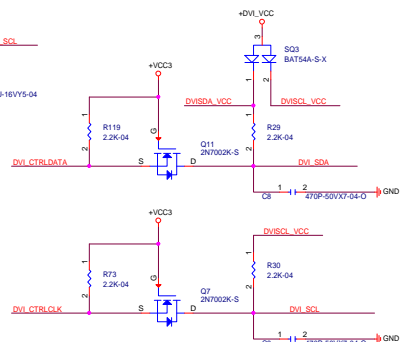
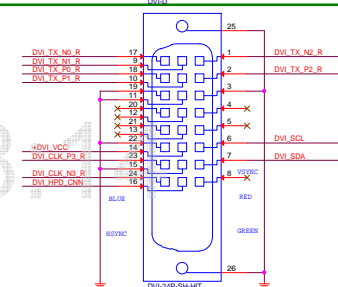
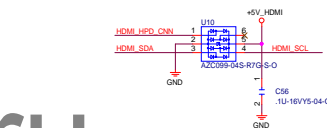
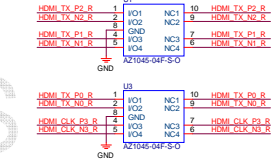
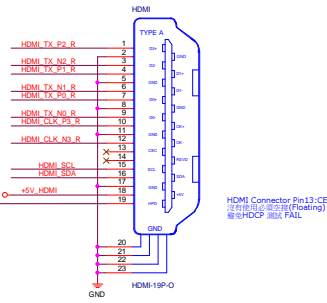
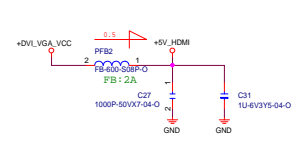
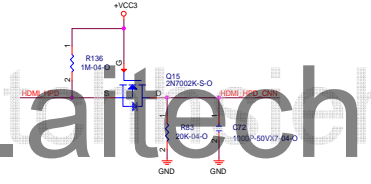
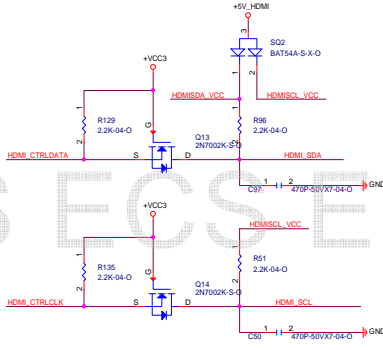
| | | | | | |
|--------------|------|---|---|-------------|-----------|
| 4 DDI2_TX_N3 | C108 | 1 | 2 | 1U-18VX7-04 | DVI_TX_P2 |
| 4 DDI2_TX_P3 | C109 | 1 | 2 | 1U-18VX7-04 | DVI_TX_N2 |
| 4 DDI2_TX_N2 | C110 | 1 | 2 | 1U-18VX7-04 | DVI_TX_P1 |
| 4 DDI2_TX_P2 | C111 | 1 | 2 | 1U-18VX7-04 | DVI_TX_N1 |
| 4 DDI2_TX_N1 | C112 | 1 | 2 | 1U-18VX7-04 | DVI_TX_P0 |
| 4 DDI2_TX_P1 | C113 | 1 | 2 | 1U-18VX7-04 | DVI_TX_N0 |
| 4 DDI2_TX_N0 | C114 | 1 | 2 | 1U-18VX7-04 | DVI_TX_P0 |
| 4 DDI2_TX_P0 | C115 | 1 | 2 | 1U-18VX7-04 | DVI_TX_N0 |



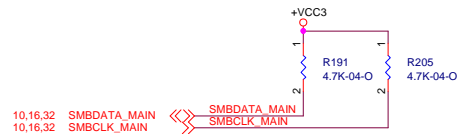
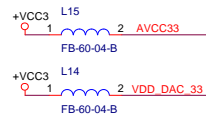
1. 16-400-900143 COMMON CHOKE 90 OHM, SMD 0805, HDMI121225F-900T04.400mA, LEAD-FREE(RoHS) TAI-TECH
2. 16-400-900171 COMMON CHOKE 90 OHM, 25%, SMD 0805, Q1CW2012H-090-1P, 300mA, LEAD-FREE(RoHS/HP) MAGIC



SDA, SCL 對地電容 - Default 先不單上件, 如 HMI 需求單上件, 請務必確認可以 Pass HDMI 的 Spec

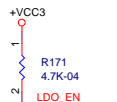


Power

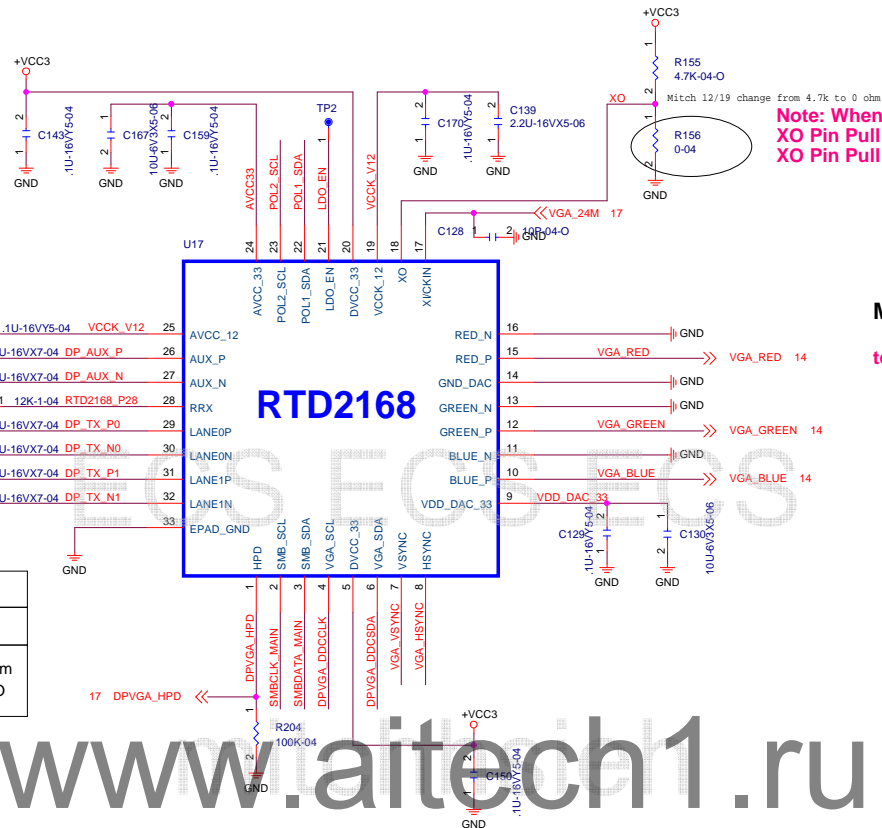


IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



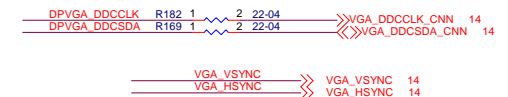
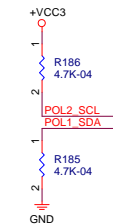
| LDO_EN(PIN21) | |
|-----------------------------|----------------------------|
| 0 | 1 |
| VCCK_V12 from External 1.2V | VCCK_V12 from Embedded LDO |



Note: When connected to non-EDID monitor,
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.
XO Pin Pull High : Enable RTD2168 embedded EDID.

Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.

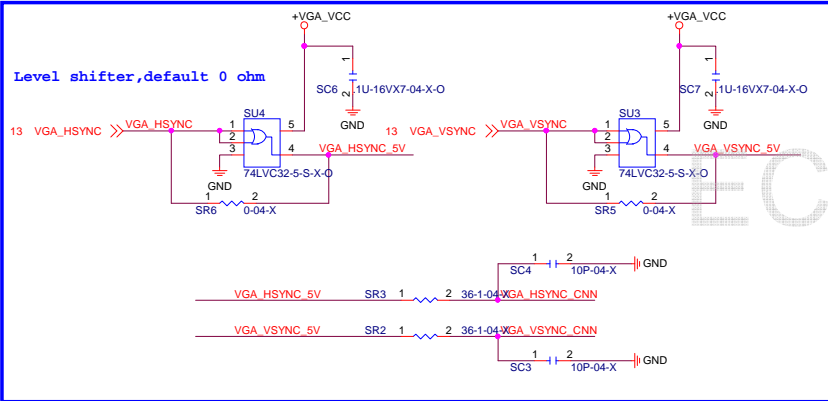
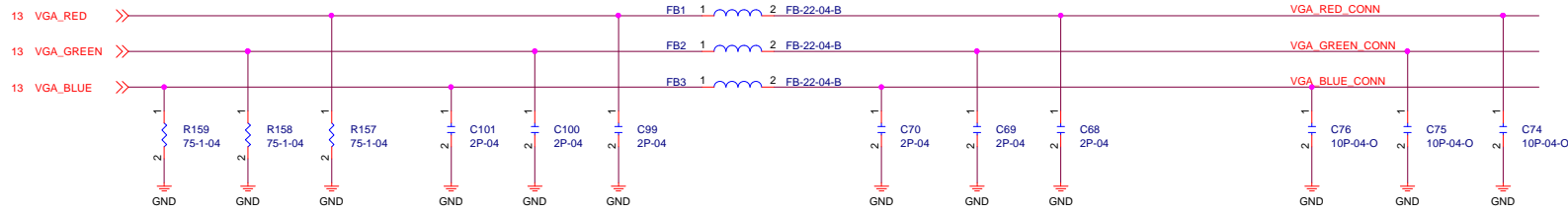


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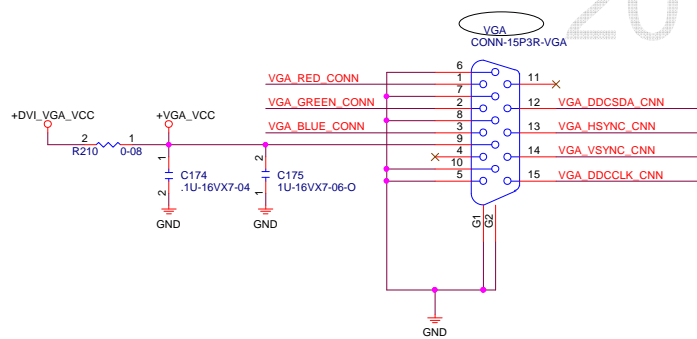
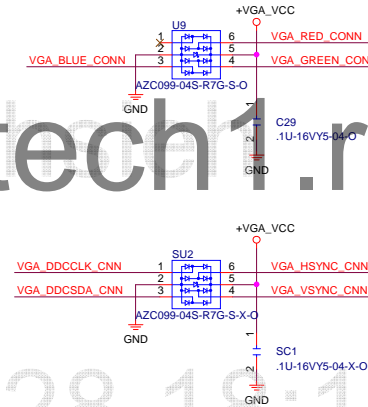
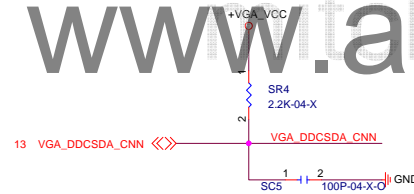
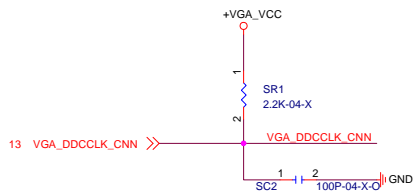
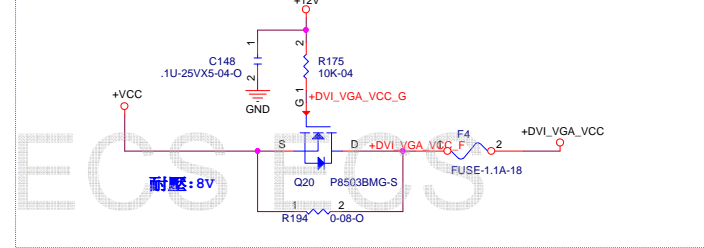
2015/07/28 18:14

VGA

Part:BLM18B220SN
P/N:16-105-220130 FB.22 OHM.25%...SMD 0402.BLM158B220SN1D.300mA...HF. LEAD-FREE.MURATA
P/N:16-105-220140 FB.22 OHM.25%...SMD 0402.FCM1005NF-220T03.300mA...HF. LEAD-FREE.TAI-TECH

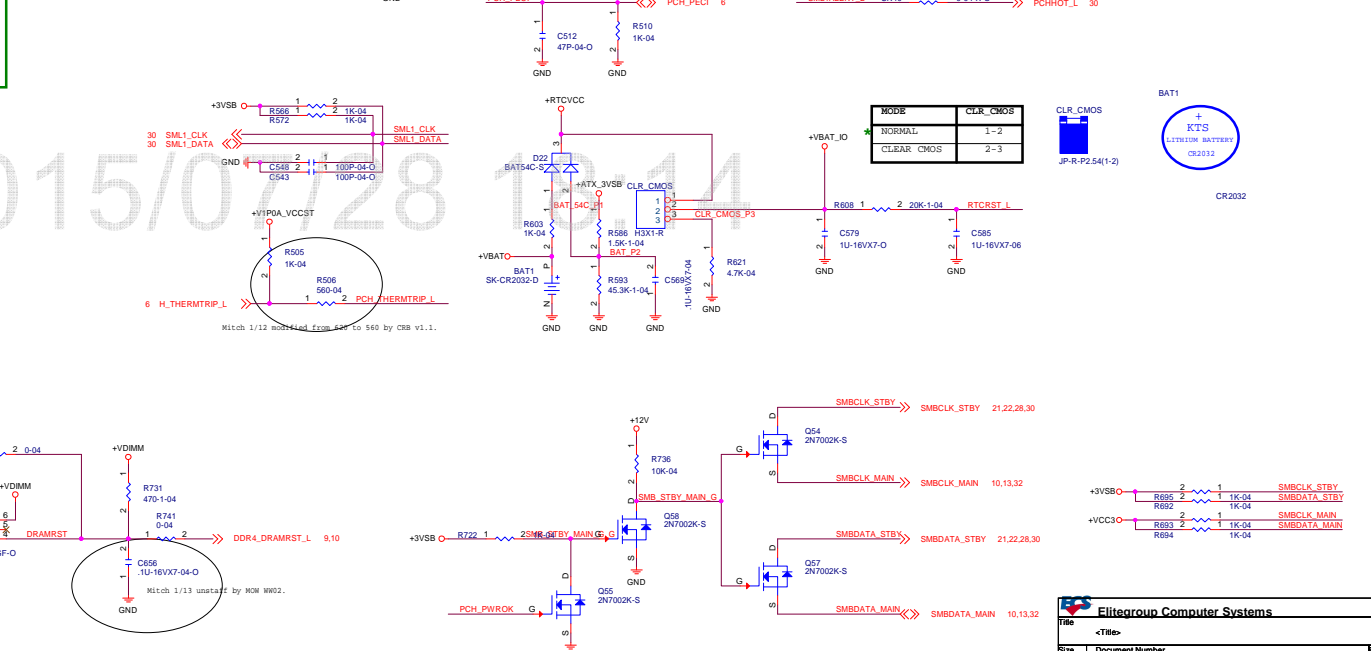
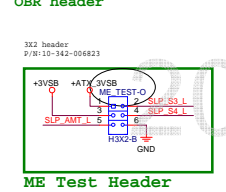
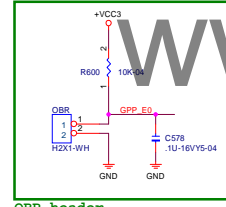
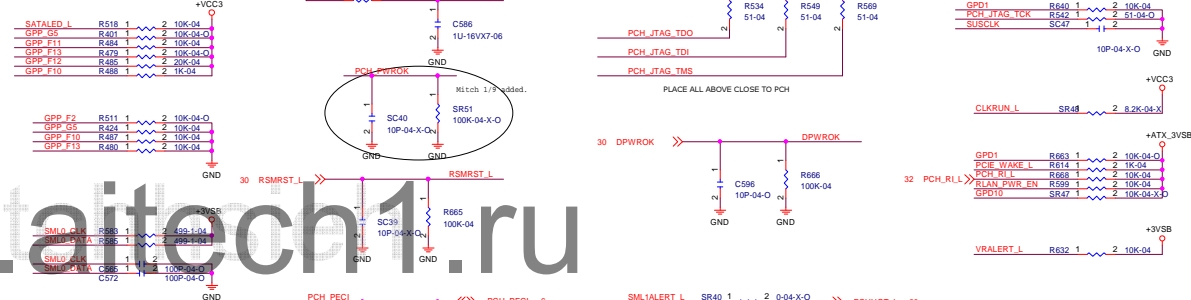


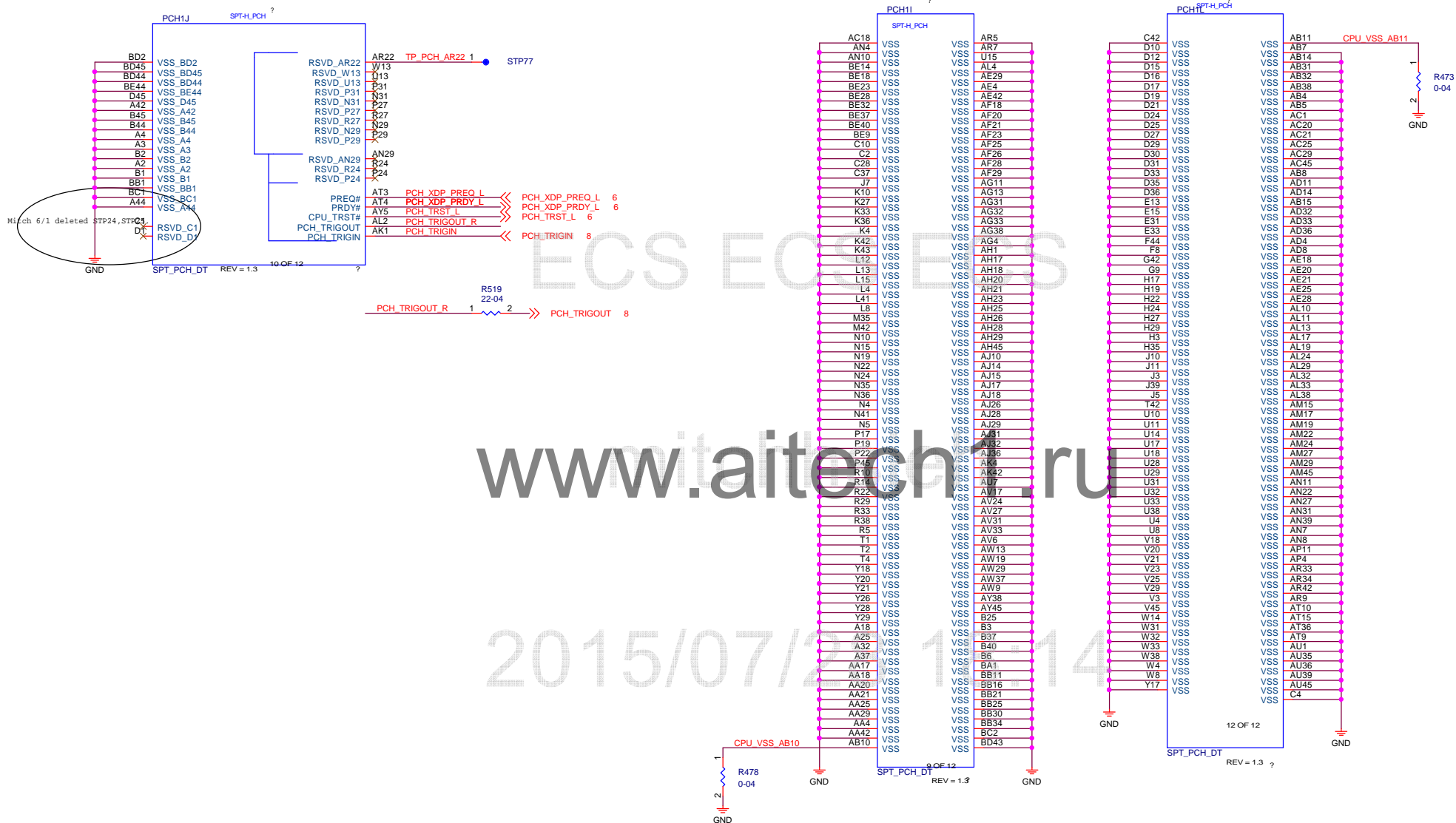
If build in Internal DVI Con, that can use the circuit to protect reverse voltage together.



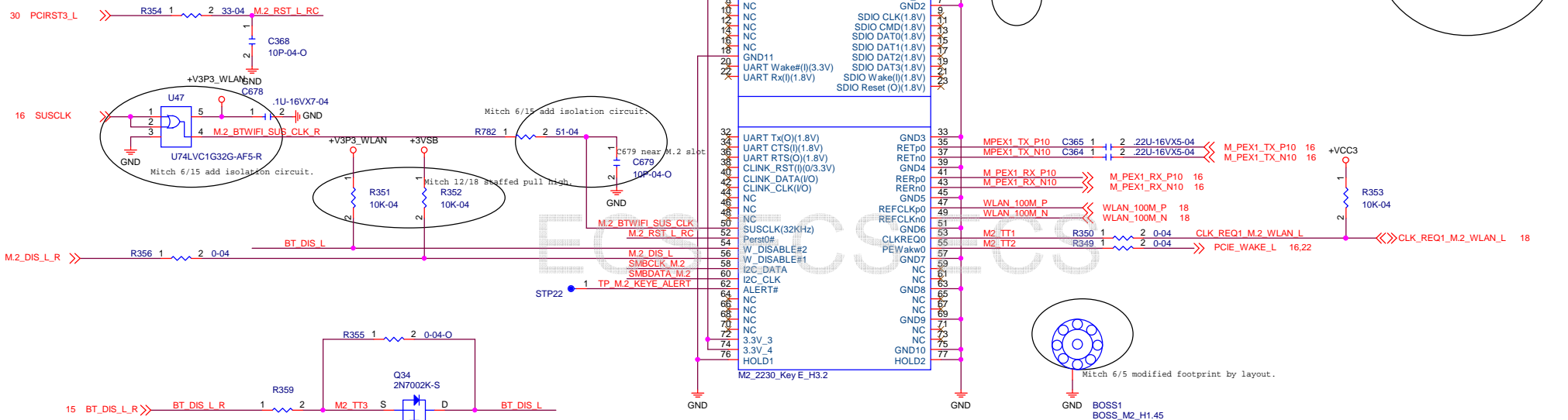
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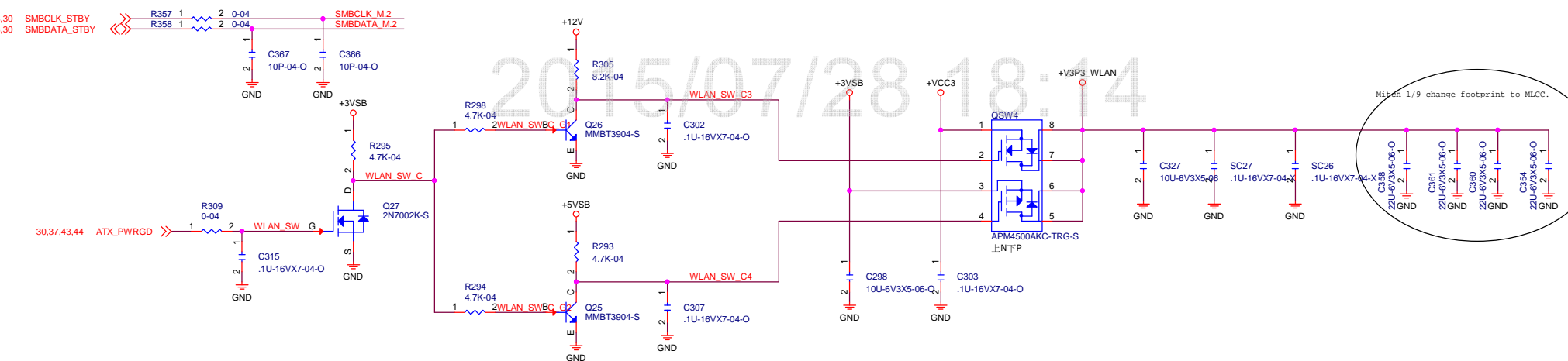
M.2 (NGFF)



0:BT DEVICE DISABLE
1:NO KILL

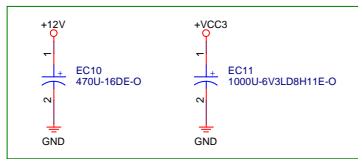
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| Key | Power Rail | Voltage Tolerance | Current Consumption Limit | |
|-----|------------|-------------------|-----------------------------|----------------------------|
| | | | Peak mA Max Avg @ 100 µs | Normal mA Max Avg @ 1 s |
| E | 3.3 V | ± 5% | 2000 | |

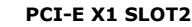


| | ATX_PWRGD | +V3P3_WLAN |
|----------|-----------|------------|
| S0 | 1 | +VCC3 |
| S3/S4/S5 | 0 | +3VSB |

```
**PCI-E SPEC**
VCC3:3A
12V:5.5A
3VSB:0.375A
```



one slot support dual lan card, reserve




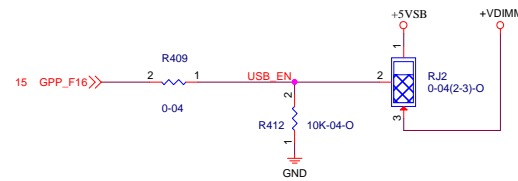
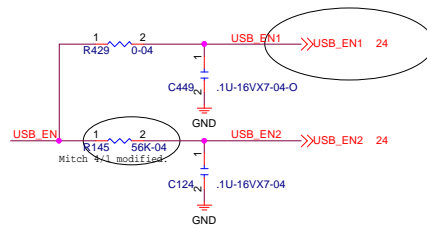
| | Ra | Rb | Rc |
|-------------------|----|----|----|
| GPIO PEG Reset | X | V | V |
| NO GPIO PEG Reset | V | X | X |

ECS ECS ECS

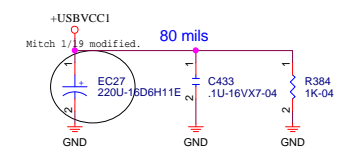
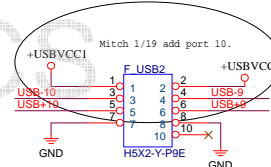
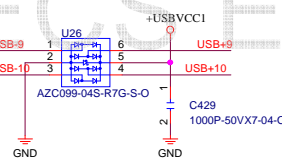
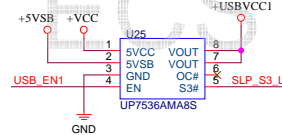
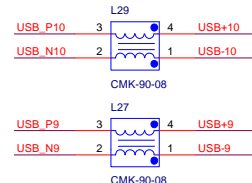
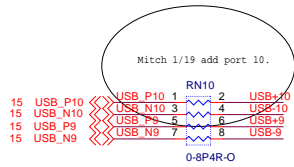
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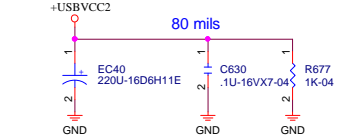
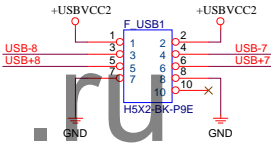
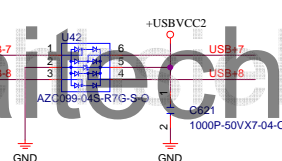
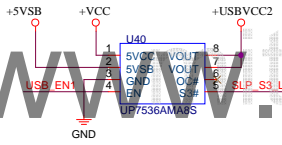
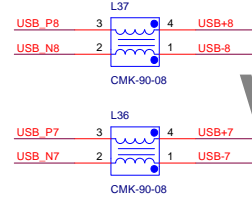
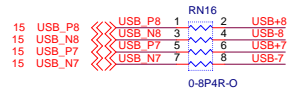
| | | |
|---|------------------------|----------------|
|  | | |
| Title | | |
| HDMI | | |
| Size | Document Number | Rev |
| Custom | H11H4-AD | 1.0 |
| Date: | Tuesday, July 14, 2015 | Sheet 23 of 46 |



| uP7536 Enable use | RJ? | RJ? | S4/S5 USB_5V_DUAL | Customer |
|-------------------|------------|-------|----------------------------|------------------------------|
| VDIMM | 0ohm (1-2) | NA | 0 Volt | Acer S4 w/o S5 w/ USB_5VDUAL |
| 5VSB | 0ohm (2-3) | NA | 5 Volt | |
| * GPIO | NA | 0 ohm | S4 : 0 Volt S5 : 5 Volt | |

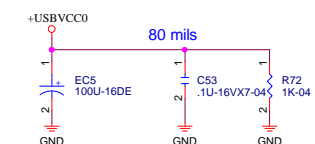
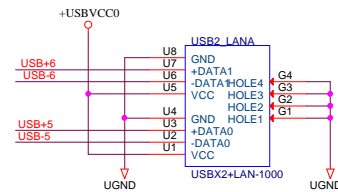
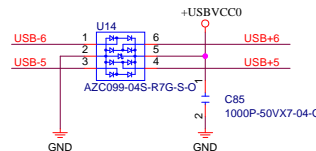
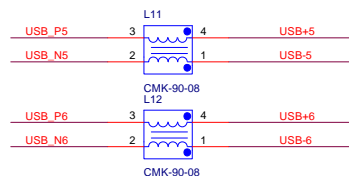
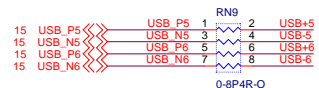


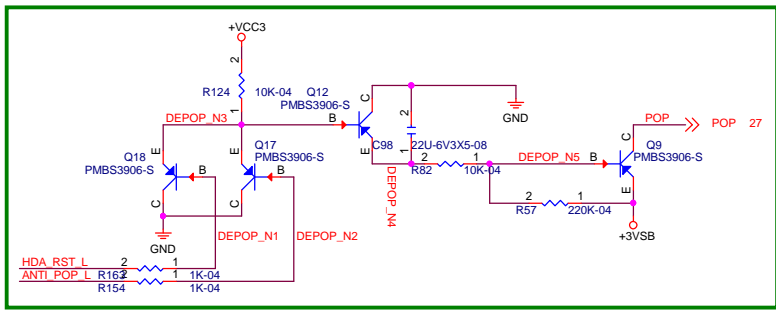
6,16,24,30,35,44 SLP_S3_L >> SLP_S3_L



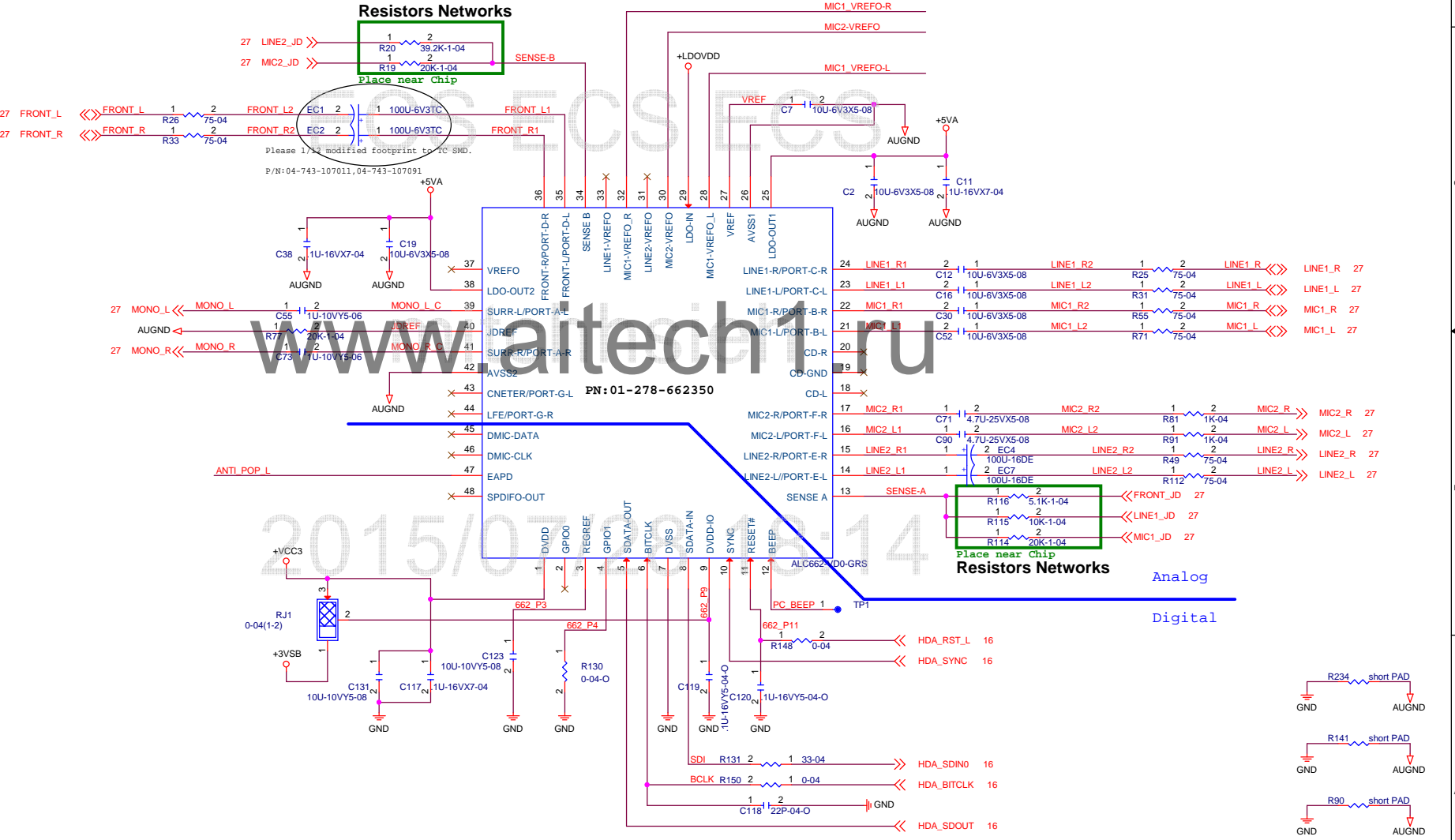
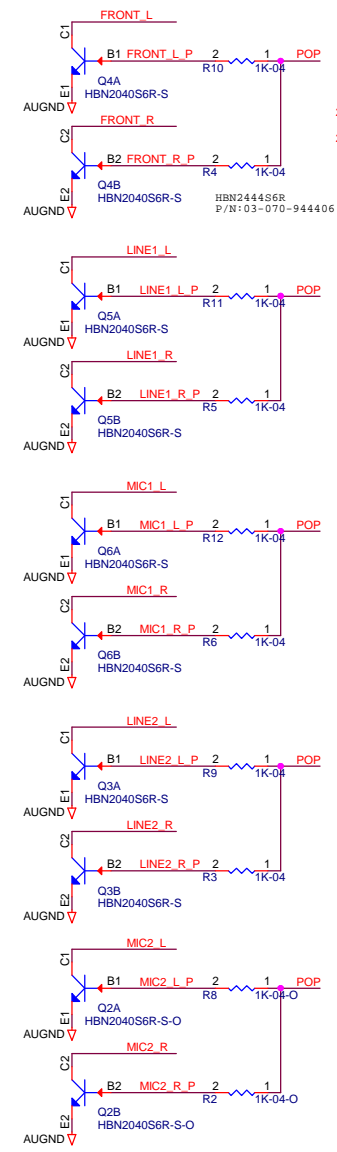
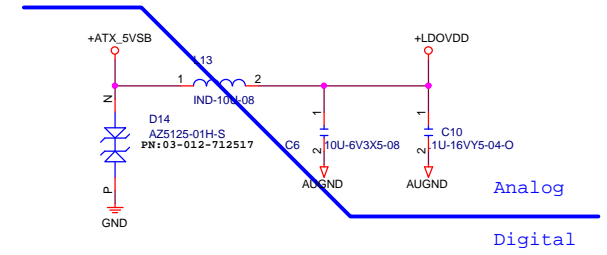
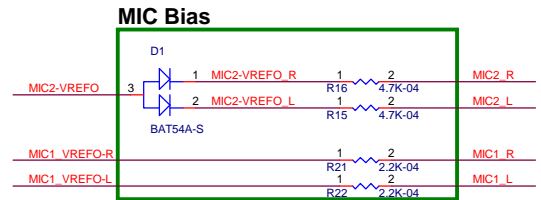
USB2.0 header

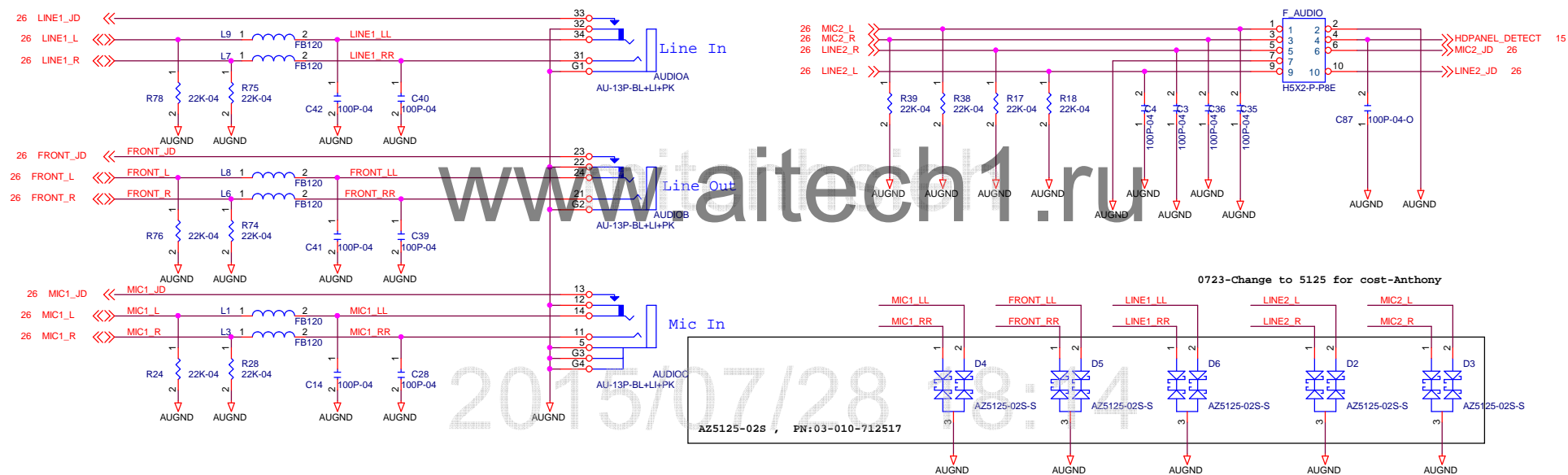
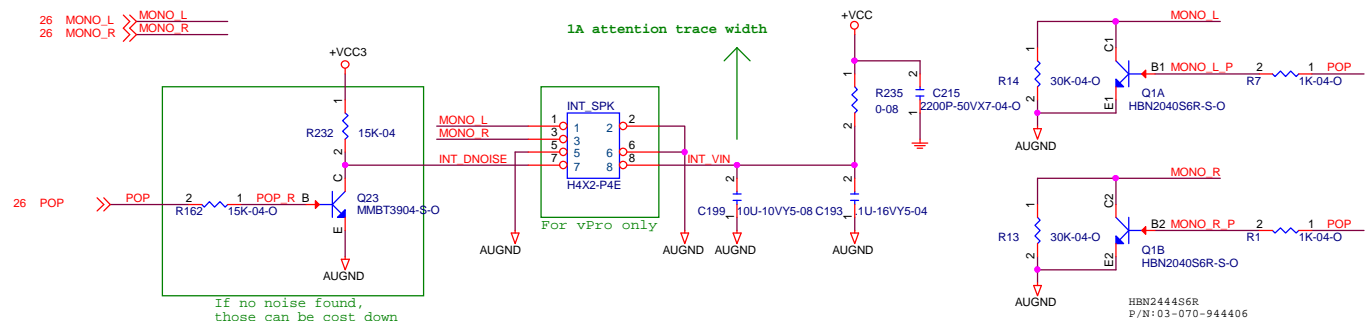
USB2.0 connector





De-pop circuit




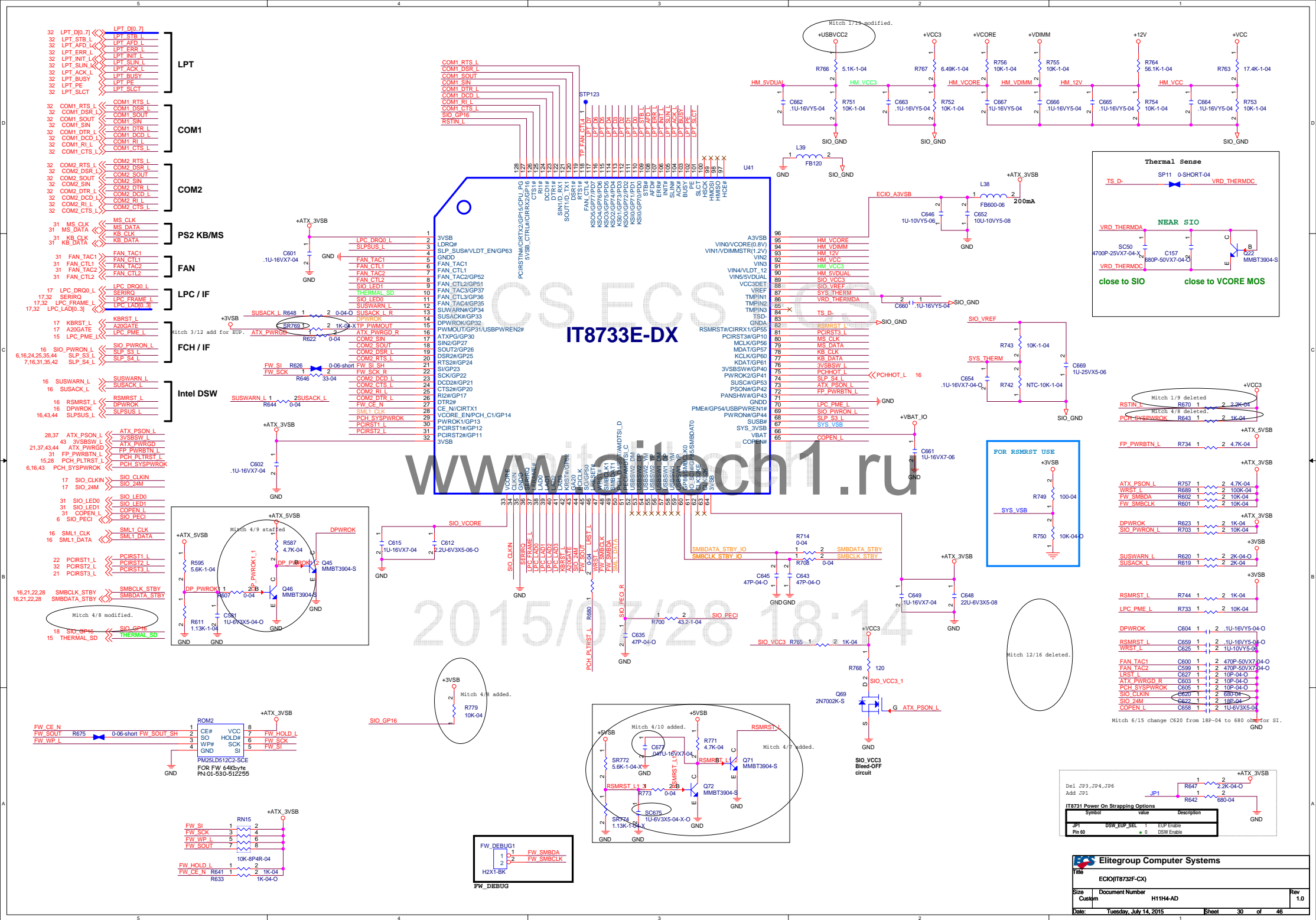


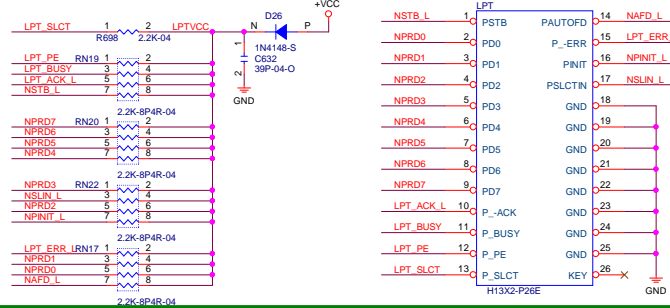
ECS ECS ECS

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| | | | |
|---|--------------------------|--|---------|
|  Elitegroup Computer Systems | | | |
| Title LAN I219LM | | | |
| Size Custom | Document Number H11H4-AD | | Rev 1.0 |
| Date: Tuesday, July 14, 2015 Sheet 29 of 46 | | | |

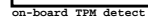




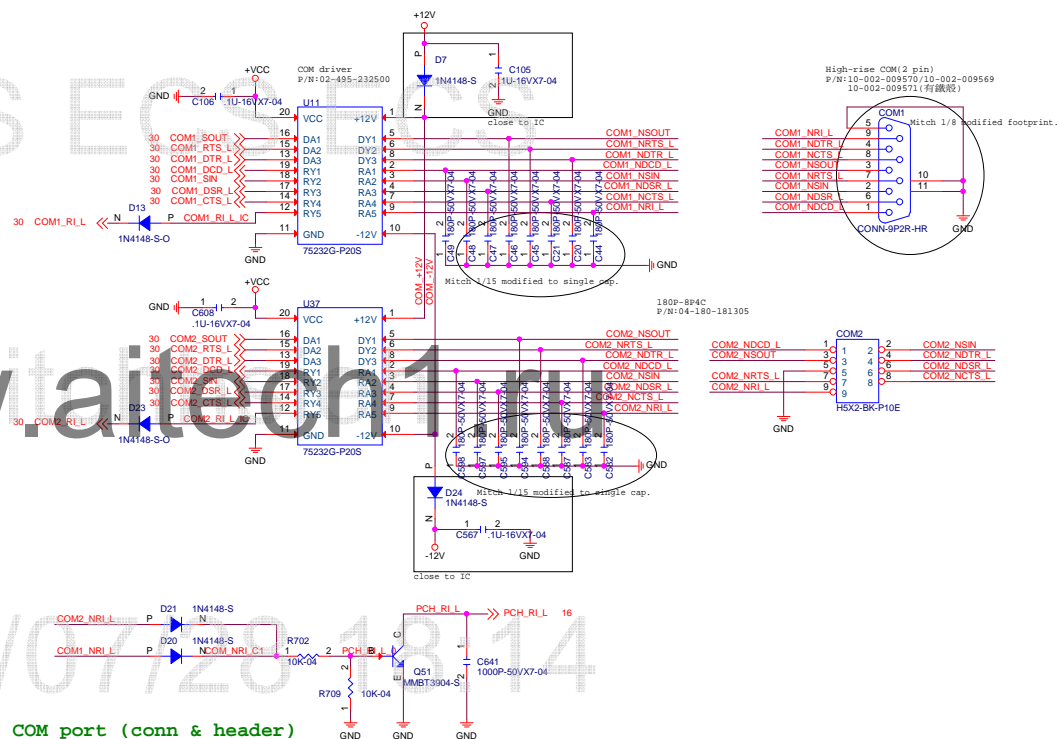
```

15  GPP_G15      << GPP_G15
17,30 LPC_LAD[0..3] <<> LPC_LAD[0..3]
17  LPCPD_L      >> LPCPD_L
17,30 SERIRQ     >> SERIRQ
17,30 LPC_FRAME_L >> LPC_FRAME_L

```



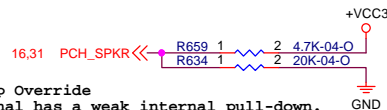
Hi with on-board TPM
Low W/O on-board TPM



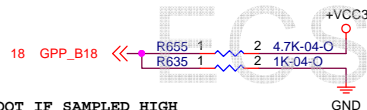
TPM chip/header circuit



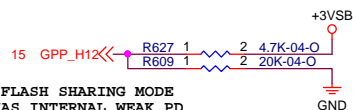
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



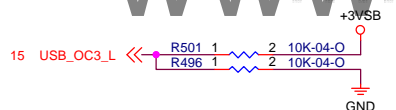
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



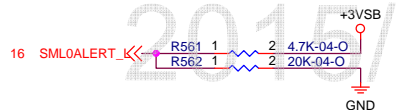
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



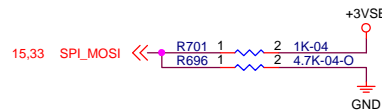
ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING



DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



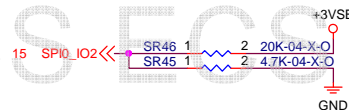
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD



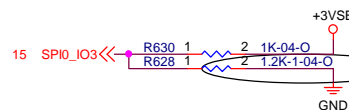
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



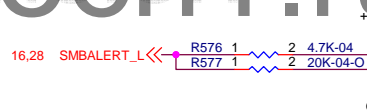
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



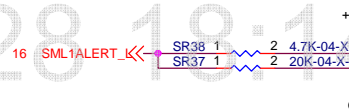
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



PERSONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1 only)



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH (DEFAULT)
PCH HAS INTERNAL WEAK PD



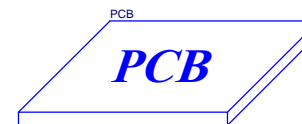
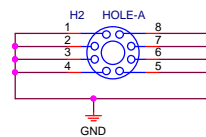
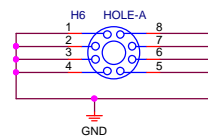
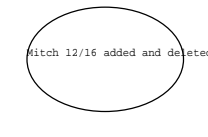
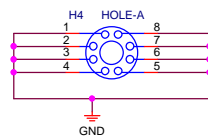
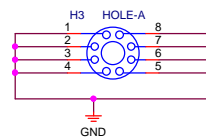
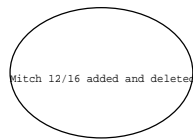
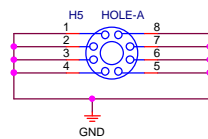
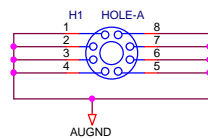
EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

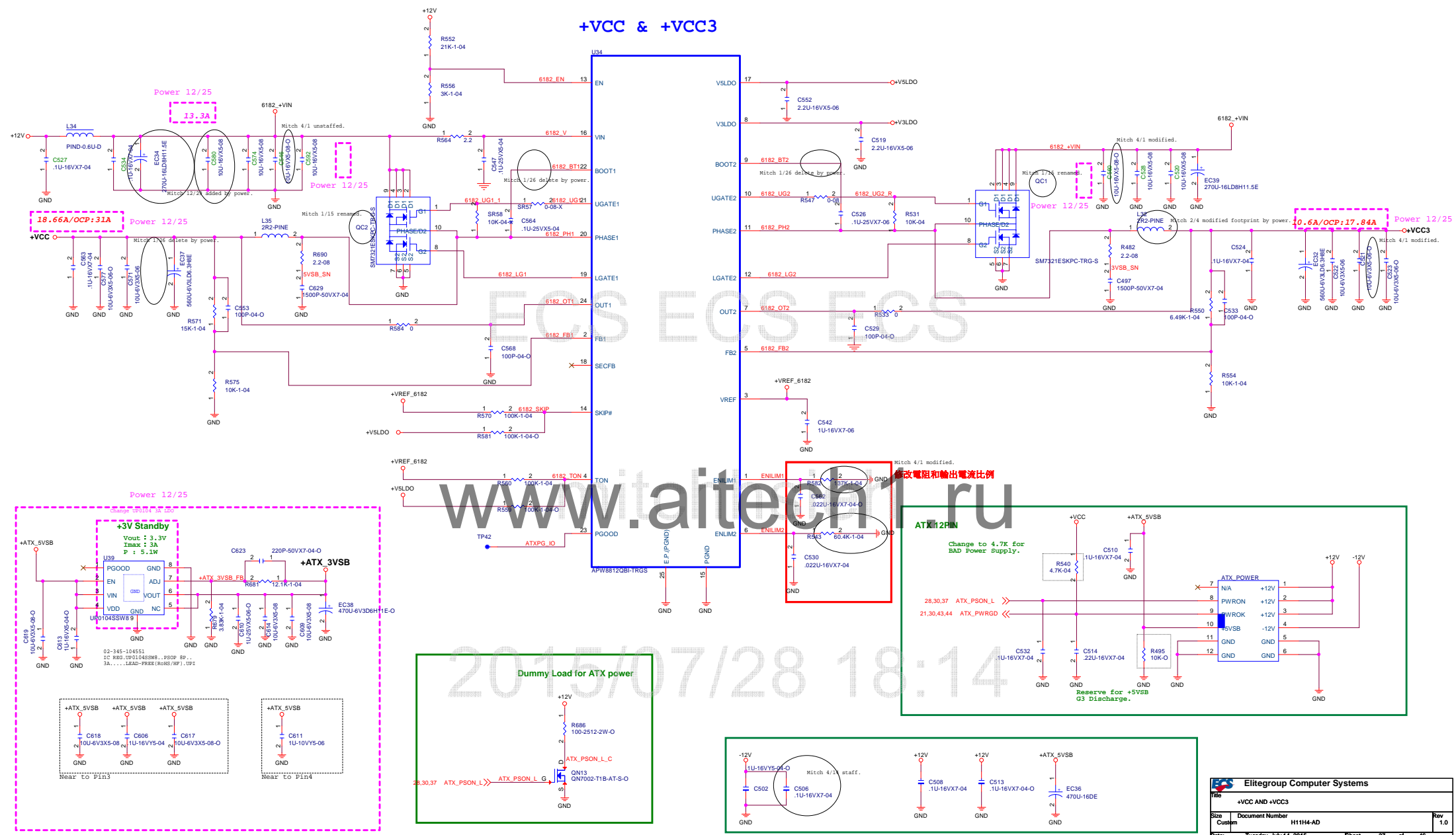
| | | | |
|--------------------|-----------------------------|-------------|------------|
| Title Strap Pin | | | |
| Size B | Document Number H11H4-AD | | Rev 1.0 |
| Date: | Tuesday, July 14, 2015 | Sheet 34 | of 46 |

ECS ECS ECS

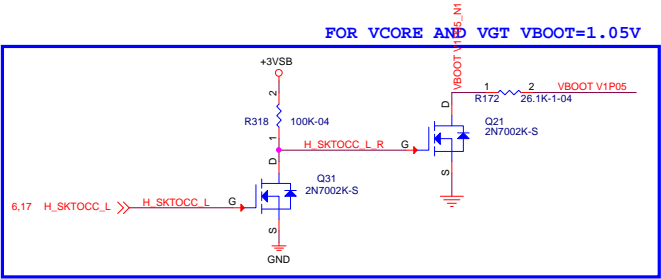
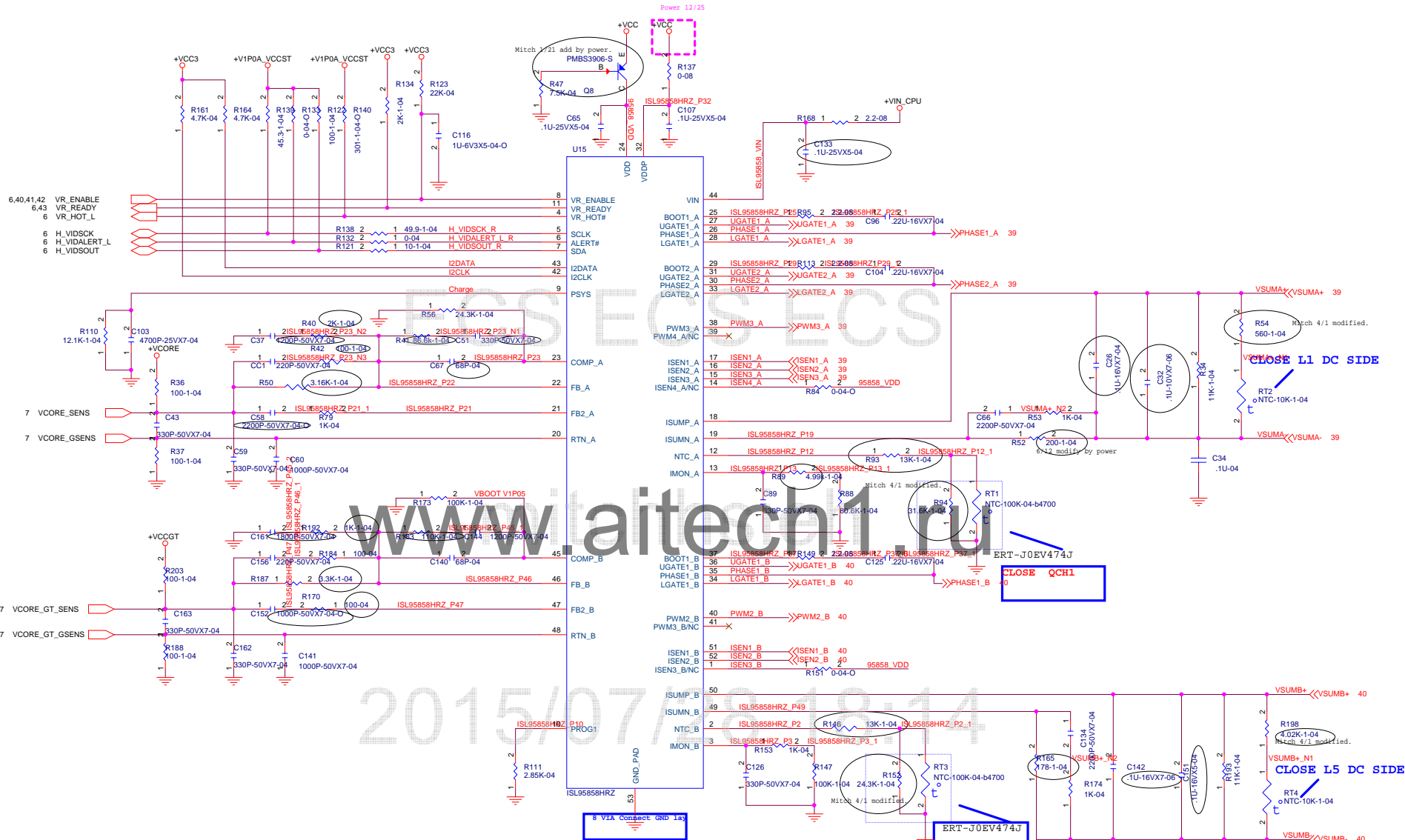
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| | | | |
|-----------------------------|------------------------|----------|----------|
| Elitegroup Computer Systems | | | |
| File | +VCC AND +VCC3 | | |
| Doc | Document Number | H11H4-AD | Rev |
| Custom | | | 1.0 |
| Date | Tuesday, July 14, 2015 | Sheet | 37 of 46 |



+V CORE_GT:
TDC/Imax : 37A/51A
OCP : 71.4A

Close VR Side

Close PWM

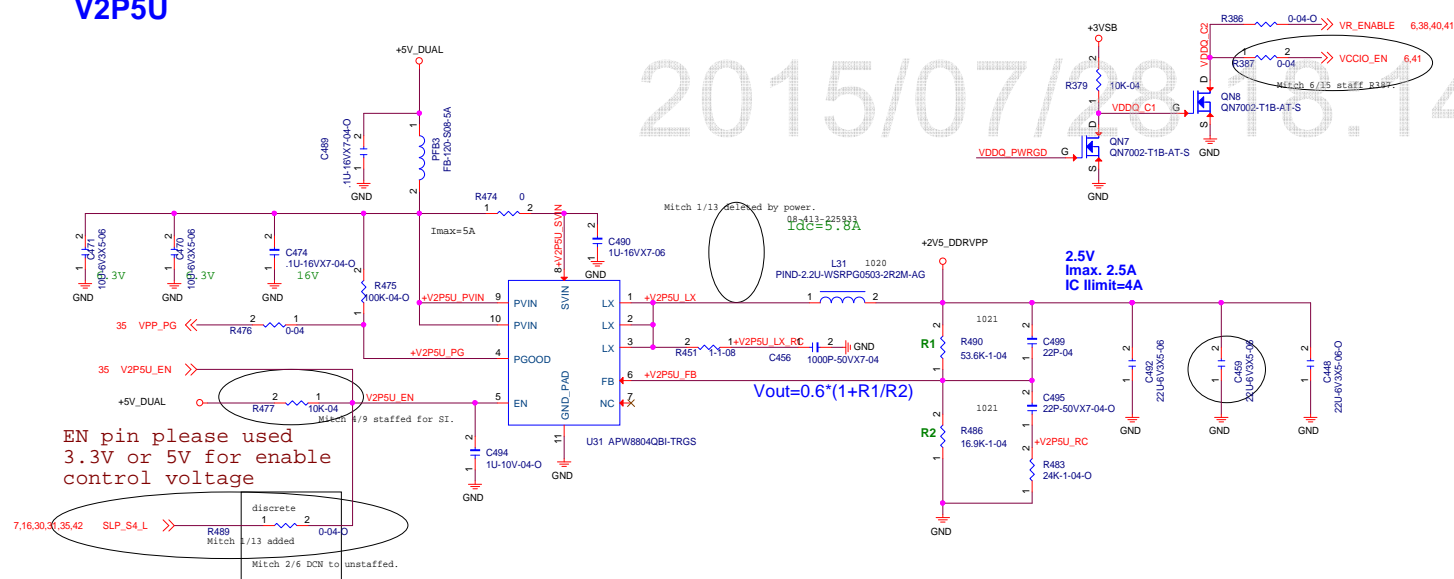
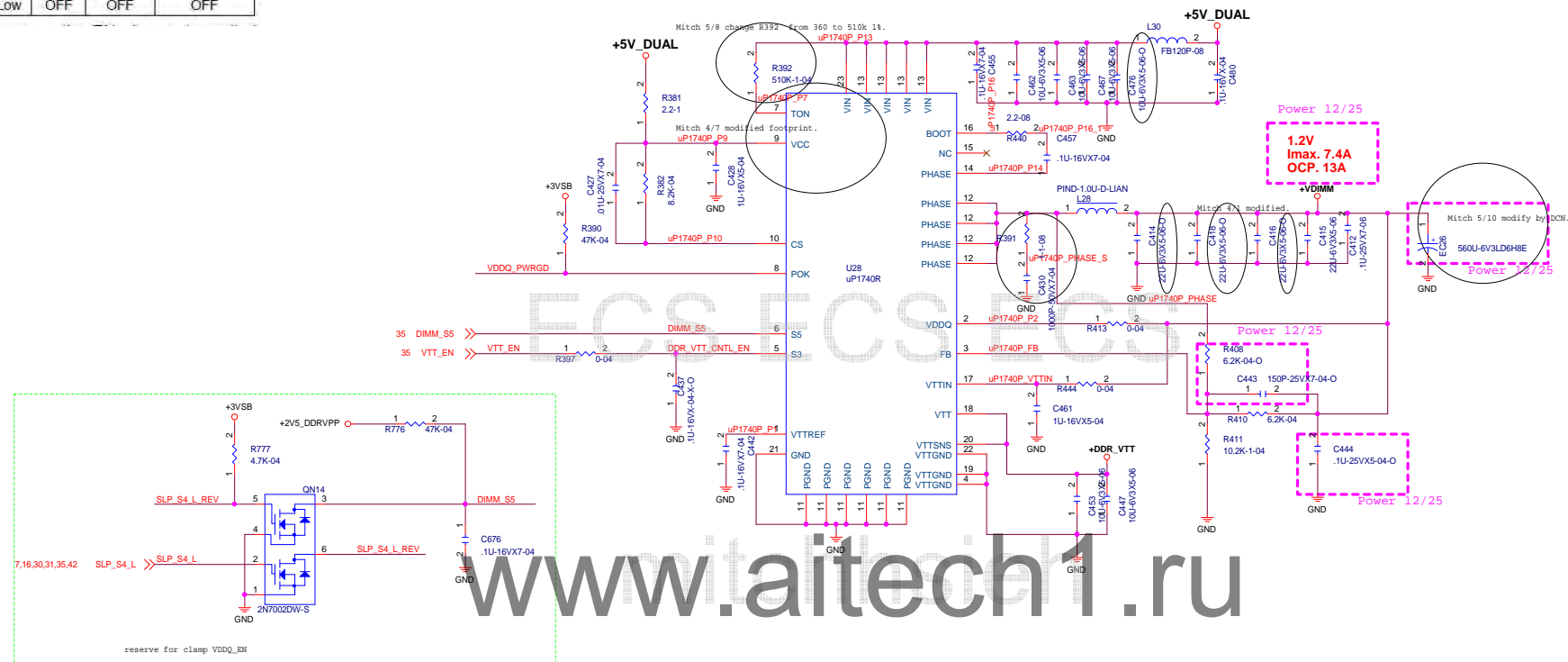
Close PWM

+VSA : 1.05V
Imax : 11.1A
OCP : 18A

Close VR Side

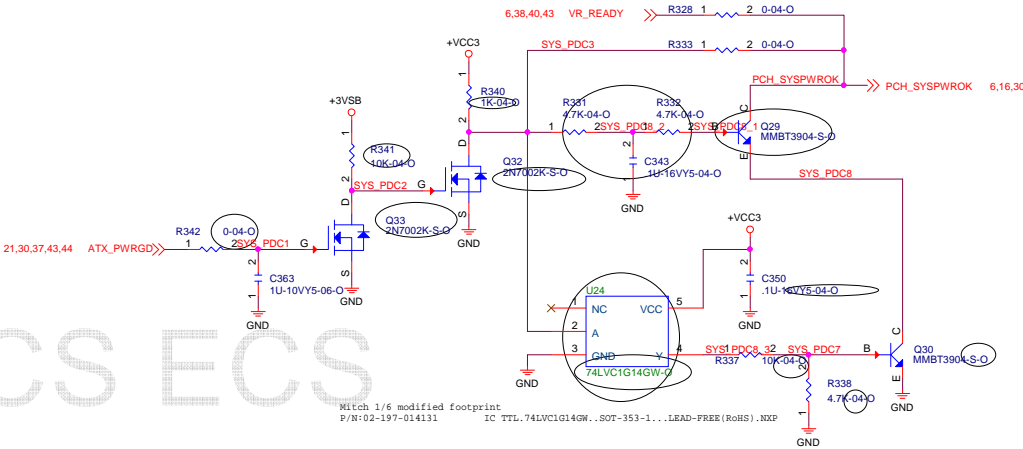
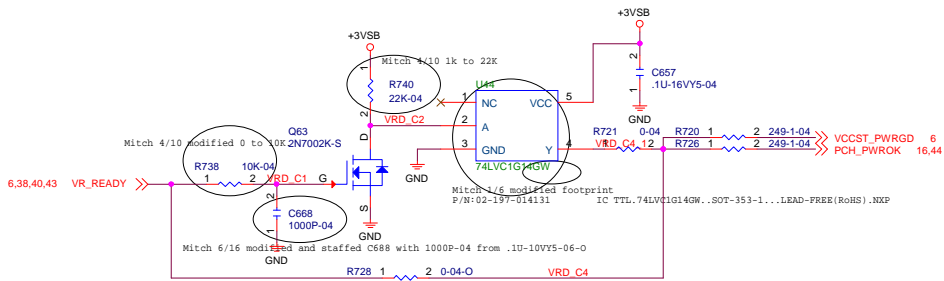
VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

| State | EN1 | EN2 | VDDQ | VTTREF | VTT |
|--------|------|------|------|--------|-------------|
| S0 | High | High | ON | ON | ON |
| S3 | Low | High | ON | ON | OFF(High-Z) |
| S4/S5 | Low | Low | OFF | OFF | OFF |
| Others | High | Low | OFF | OFF | OFF |

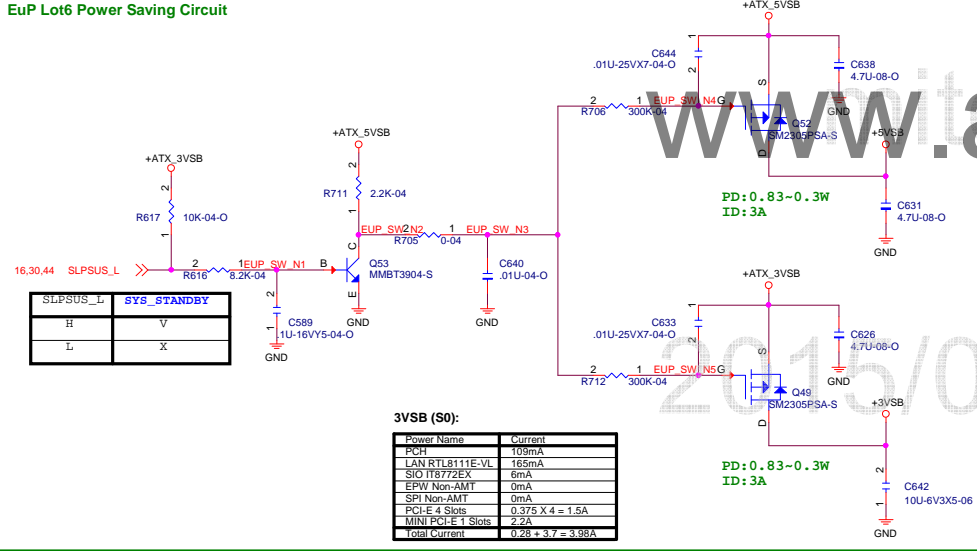


SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS

PCH & VCCST PWROK

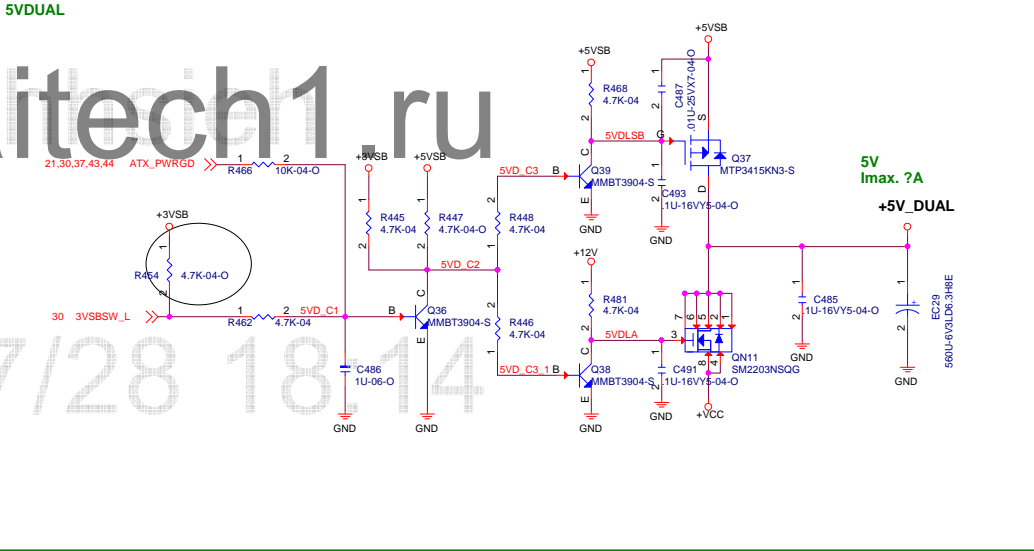


EuP Lot6 Power Saving Circuit



| 3VSB (S0): | |
|--------------------|--------------------|
| Power Name | Current |
| PCH | 109mA |
| LAN RTL8111E-VL | 165mA |
| SIO I18772EX | 6mA |
| EPW Non-AMT | 0mA |
| SPI Non-AMT | 0mA |
| PCI-E 4 Slots | 0.375 X 4 = 1.5A |
| MINI PCI-E 1 Slots | 2.2A |
| Total Current | 0.28 + 3.7 = 3.98A |

5VDUAL

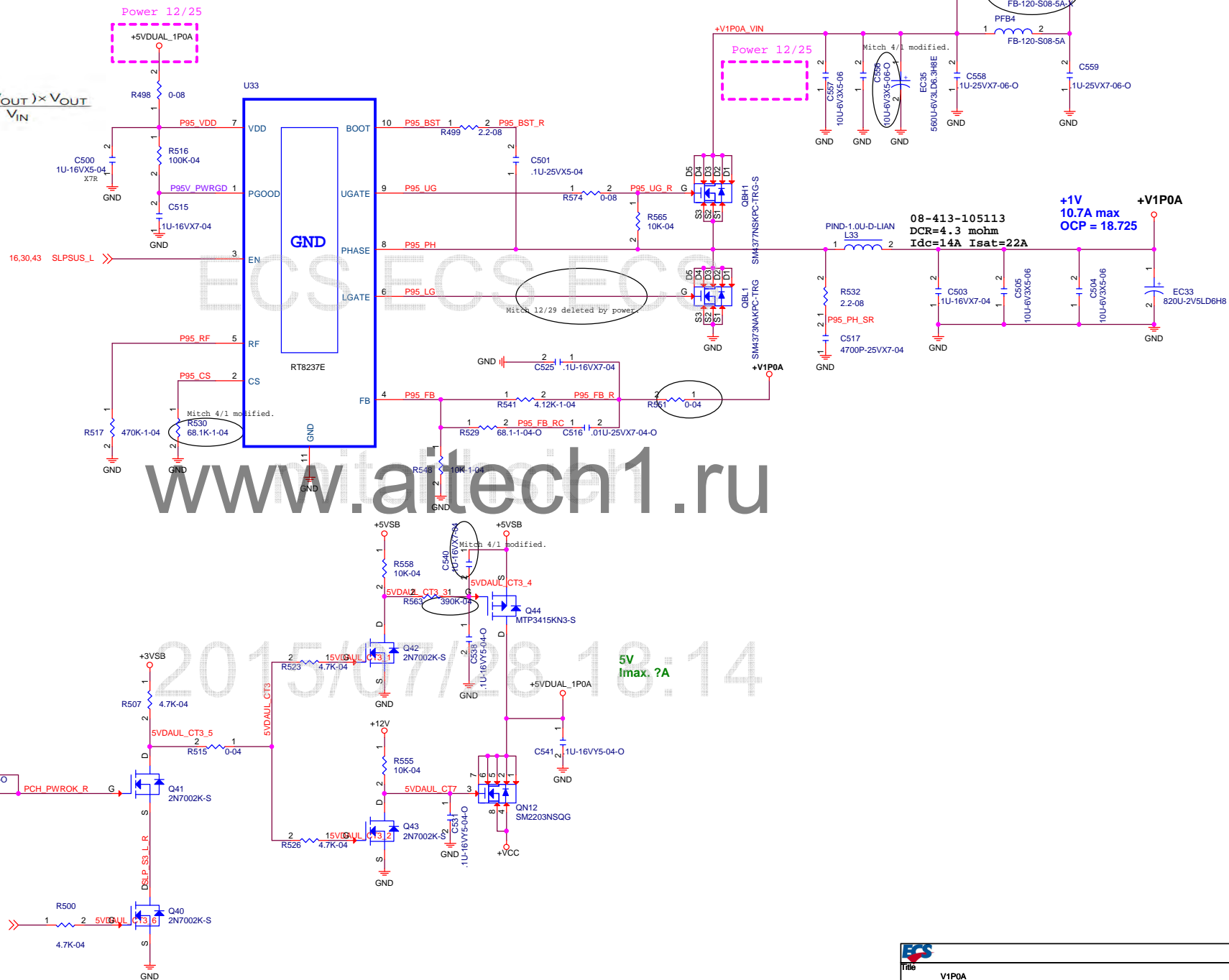


| Title | | | |
|------------------------|--|-----------------|--|
| DC/DC DDRVPP & 5VDUAL | | | |
| Size | | Document Number | |
| Custom | | H11H4-AD | |
| Date: | | Rev | |
| Tuesday, July 14, 2015 | | 1.0 | |
| Sheet | | of | |
| 43 | | 46 | |

V1P0A

$$I_{LOAD_OC} = \frac{V_{CS_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{CS_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



| | | | |
|--------|------------------------|----------|----------|
| Title | | | V1P0A |
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| ATX Single P/S | | |
|----------------|-------|-------|
| 5VSB | 12V | -12V |
| +/-5% | +/-5% | +/-5% |

| ATX4P | |
|-------|-------|
| 12V | +/-5% |

| Switching ISL95855 | |
|--------------------|-----|
| 70A | 37A |
| 10A | |

| Switching APW8727L | |
|--------------------|--|
| 5.5A | |

| Intel SkyLake CPU | | |
|-------------------|-------|----------|
| VCORE | SVID | 79A(65W) |
| VCC_GT | SVID | 51A |
| VCC_SA | 0.95V | 11.1A |
| VCCIO | 0.95V | 5.5A |
| VDIMM | 1.2V | 2.8A |

| Intel SKT-PCH (Q170/B150) | | |
|---------------------------|------|--------|
| VCCPRIM_1p0 | 1V | 6.15A |
| VCCCLK1 | 1V | 0.035A |
| VCCCLK2 | 1V | 0.204A |
| VCCCLK3 | 1V | 0.058A |
| VCCCLK4 | 1V | 0.036A |
| VCCCLK5 | 1V | 0.008A |
| VCCMPHY_1p0 | 1V | 4.09A |
| VCCHDAPLL_1p0 | 1V | 0.008A |
| VCCMPHYPLL_1p0 | 1V | 0.025A |
| VCCPCIE3PLL_1p0 | 1V | 0.037A |
| VCCUSB2PLL_1p0 | 1V | 0.013A |
| VCCPGPPA | 3.3V | 0.088A |
| VCCPGPBCH | 3.3V | 0.273A |
| VCCPGPPD | 3.3V | 0.106A |
| VCCPGPEF | 3.3V | 0.141A |
| VCCPGPPG | 3.3V | 0.132A |
| VCCSPI | 3.3V | 0.013A |
| VCCATS | 3.3V | 0.007A |
| VCCFDA | 3.3V | 0.075 |
| VCCPRIM_3p3 | 3.3V | 0.370 |
| VCCDSW_3p3 | 3.3V | 0.502A |
| VCCRTCPRIM_3p3 | 3.3V | 0.001A |
| VCCRTC | 3.0V | 0.001A |

| DDR4 DIMM 1600MHz (2) | | |
|-----------------------|------|-------------|
| VDIMM | 1.2V | 1.53A (TDC) |
| VDIMM_VTT | 0.6V | 0.6A |
| VPP | 2.5V | 1.12A |

Mitch 3/25 update for Hynix UDIMM.

| SATA power per | |
|----------------|------|
| 12V | 1.2A |
| 5V | 1.6A |

Total 2 connector

| Switching APW8727L | |
|--------------------|-------|
| 2.66A | V1P0A |

$$I_{in} = ((I_{out} * V_{out}) / 0.8) / V_{in}$$

| LDO V_3P3_LAN | | |
|---------------|------|-------|
| VDD3P3 | 3.3V | 177mA |
| VDD10 | 1V | 300mA |

| LAN | | |
|--------|------|-------|
| VDD3P3 | 3.3V | 177mA |
| VDD10 | 1V | 300mA |

| FAN | | |
|---------|------|----|
| CPU_FAN | +12V | 1A |
| SYS_FAN | +12V | 1A |

| VGA | |
|-----|------|
| 5V | 0.5A |
| DVI | |
| 5V | 0.5A |

| SIO IT8733 | | |
|--------------|------|-----|
| 3VSB | 3.3V | TBD |
| VCC3 | 3.3V | TBD |
| Battery 3.3V | 3.3V | TBD |

| AUDIO ALC662-VD | | |
|-----------------|------|------|
| DVDD 3.3V | 3.3V | 11mA |
| AVDD | 5V | 42mA |
| Internal LDO | | |



| Title | | |
|------------------------|----------|---------|
| Power Delivery | | |
| Size | | |
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